USER MANUAL

Accessory 51E

UMAC 4096 Interpolator

3Ax-603438-xUxx

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DELTA TAU
Data Systems, Inc.

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INTRODUCTION

Overview

Delta Tau's ACC-51E UBUS Interpolator Accessory is a sine wave input interpolator designed to interface 2 (optionally 4) analog quadrature encoders to Delta Tau Data System's UBUS Euro card style devices.

The ACC-51E is a 3U size card that mounts in the same racks as Delta Tau's Turbo UMAC or MACRO station processors.

Features

The Interpolator accepts inputs from two (optionally 4) sinusoidal or quasi-sinusoidal encoders and provides encoder position data to the motion processor. This interpolator creates 4,096 steps per sine-wave cycle.

The Interpolator can accept a voltage-source (1Vp-p) signal from the encoder. A jumper selects between unterminated or 120Ω input termination.

The maximum sine-cycle frequency input is approximately 1.4MHz, which gives a maximum speed of about 5.734 billion steps per second.

When used with a 1000 line sinusoidal rotary encoder, there will be 4,096,000 discrete counts per revolution (128,000 whole counts). The maximum calculated electrical speed of this encoder would be 1,400 RPS or 84,000 RPM, which exceeds the maximum physical speed of most encoders.

The interpolator is a UBUS product that has a Euro card connector that allows it to be placed in the same rack as a UMAC or MACRO station processor.

The ACC-51E is a CS2 or CS3 device in the UBUS backplane. Therefore the memory map for this card is similar to the ACC24E2x style axis cards.

Limitations When Used With UMAC MACRO Station

The UMAC MACRO Station has been designed as an 8-axis device. The ACC-51E occupies the same backplane select lines as ACC24E2 style axis cards and gets configured using the same I-VARs that a typical MACRO Station uses. Therefore, the ACC-51E occupies a minimum of 4 axes in the MACRO station application.

If there are more than 4 motors to be configured in the UMAC MACRO system, special consideration must be made to incorporate the ACC-51E into the system. The use of "stack" style axis cards allows the UMAC MACRO Station rack to contain more than 8 axes of addressable space. When configured this way, the user must put setup values into the gate array that is located inside the ACC-51E card.

Board Configuration

Base Configuration

The base version of the ACC-51E consists of a 3U size board with:

2 - sinusoidal encoder inputs each individually configurable to accommodate 1V p-p sinusoidal encoders.

Options

OPT 1	301-603195-OPT	Additional 2 Axes (Axis 3 & 4)
OPT 2	302-603195-OPT	Hiperface Interface

Option 1:
Provides the interface circuitry and connectors for 2 additional sinusoidal encoders, for a total of four encoders on the ACC-51E.

Option 2:
Provides the on-board circuitry to read the absolute position of Stegmann SINCOS® and SINCODER® encoders using their digital interface, "HIPERFACE®".

NOTE

The options described above must be installed at the factory.

Indicators

Please refer to the layout diagram of the UBUS interpolator for the location of the indicators on the board.

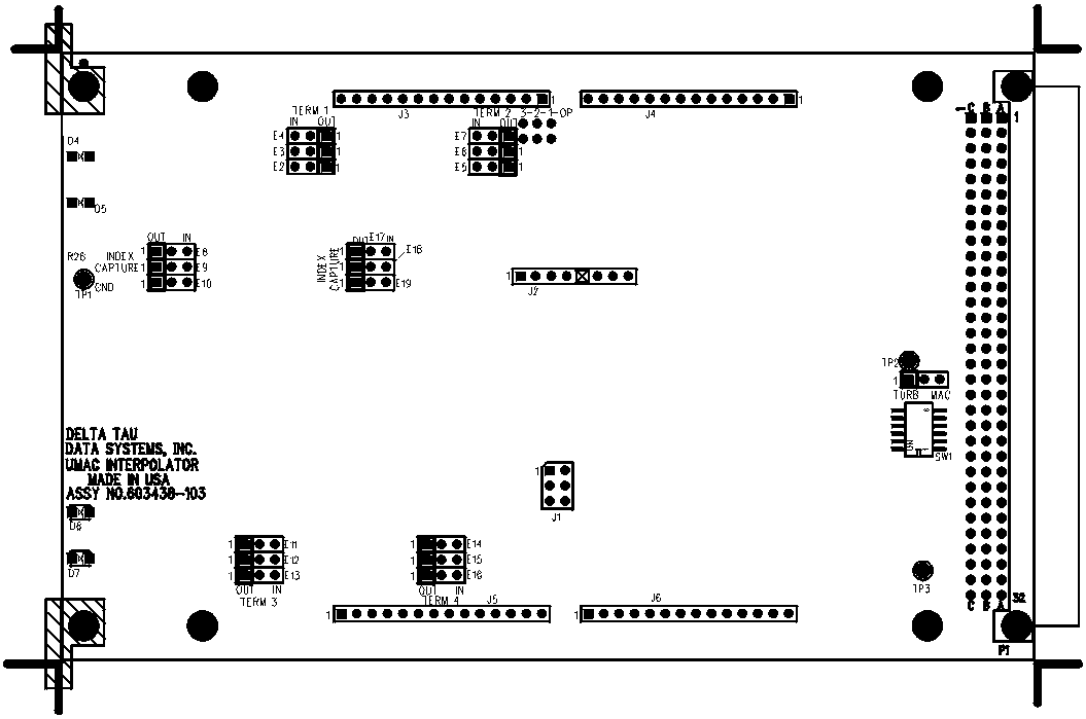
D4, D5, {D6, D7 Opt 1} AQUAD Indicators

These LED's indicate the A-channel quadrature input. When the encoder is operating normally, this indicator will flicker with a rate that is dependent upon the speed of the moving encoder.

D4 is input #1, D5 is input #2. With ACC-51E opt 1 D6 is input #3, D7 is input #4.

LAYOUT OF ACC-51E, UBUS INTERPOLATOR

Below you will find a diagram showing Jumpers and connectors on the ACC-51E (rev 3).



Dipswitch & E1 Jumper Configuration

S1 is a 6-point dipswitch that determines how the ACC-51E is to be mapped to a Turbo UMAC processor or MACRO station processor.

Jumper E1 selects between MACRO station and Turbo UBUS backplane addressing.

On backplanes that are using addressable slots, all dipswitch positions should be left in the "ON" position.

On non-addressed backplanes, the user must select addressing.

There are two addressing schemes that are used depending upon the type of UMAC Processor. The UMAC TURBO Processor table is shown followed by the table used by the UMAC MACRO Station processor.

ACC-51E MAPPINGS WHEN USED WITH UMAC TURBO CPU

The table below shows the addresses and switch settings used for the Turbo UMAC models:

ACC-51E MAPPING TABLE
{CS2, CS3 MAPPINGS WHEN USED WITH UMAC TURBO CPU}

Interp SW1 Settings						Turbo PMAC Servo IC # (m)	1st Channel	2nd Channel	3rd Channel	4th Channel	I-vars	CS16 Ident. Address
6	5	4	3	2	1							
on	on	on	on	on	on	2	$78200	$78208	$78210	$78218	I7200-I7249	$78F08
on	on	on	on	on	off	3	$78300	$78308	$78010	$78318	I7300-I7349	$78F0C
on	on	on	off	on	on	4	$79200	$79208	$79210	$79218	I7400-I7449	$79F08
on	on	on	off	on	off	5	$79300	$79308	$79310	$79318	I7500-I7549	$79F0C
on	on	off	on	on	on	6	$7A200	$7A208	$7A210	$7A218	I7600-I7649	$7AF08
on	on	off	on	on	off	7	$7A300	$7A308	$7A310	$7A318	I7700-I7749	$7AF0C
on	on	off	off	on	on	8	$7B200	$7B208	$7B210	$7B218	I7800-I7849	$7BF08
on	on	off	off	on	off	9	$7B300	$7B308	$7B310	$7B318	I7900-I7949	$7BF0C
on	on	on	on	off	on	2*	$78220	$78228	$78230	$78238	I7250-I7259	$78F28
on	on	on	on	off	off	3*	$78320	$78328	$78030	$78338	I7350-I7359	$78F2C
on	on	on	off	off	on	4*	$79220	$79228	$79230	$79238	I7450-I7459	$79F28
on	on	on	off	off	off	5*	$79320	$79328	$79330	$79338	I7550-I7559	$79F2C
on	on	off	on	off	on	6*	$7A220	$7A228	$7A230	$7A238	I7650-I7659	$7AF28
on	on	off	on	off	off	7*	$7A320	$7A328	$7A330	$7A338	I7750-I7759	$7AF2C
on	on	off	off	off	on	8*	$7B220	$7B228	$7B230	$7B238	I7850-I7859	$7BF28
on	on	off	off	off	off	9*	$7B320	$7B328	$7B330	$7B338	I7950-I7959	$7BF2C

The memory mapping for Turbo UMAC models allows for a total of 64 encoder channels to be selected. The dipswitch selects between any of the 16 banks of memory. This allows for up to 16 ACC-51Es to be logically configured.

NOTE

The ACC-51E defines the mapping for its encoder channels as the same as the mapping for other devices that provide encoder inputs. Therefore, although there are 16 - four channel memory "slots" to place the ACC-51E into, these same "slots" are shared with the axis cards.

ACC-51E MAPPINGS WHEN USED WITH UMAC MACRO STATION CPU

The table below shows the addresses and switch settings used for the UMAC MACRO STATION:

ACC-51E MAPPING TABLE
{CS2, CS3 MAPPINGS WHEN USED WITH UMAC MACRO STATION CPU}

Backplane Slot Number	Interp SW1 Settings						1st Channel	2nd Channel	3rd Channel	4th Channel
	6	5	4	3	2	1				
1	off	off	off	off	on	on	$C040	$C048	$C050	$C058
2	off	off	off	off	off	off	$C060	$C068	$C070	$C078
3	off	off	off	off	on	on	$C040	$C048	$C050	$C058
4	off	off	off	off	off	off	$C060	$C068	$C070	$C078
5	off	off	off	off	on	on	$C040	$C048	$C050	$C058
6	off	off	off	off	off	off	$C060	$C068	$C070	$C078
7	off	off	off	off	on	on	$C040	$C048	$C050	$C058
8	off	off	off	off	off	off	$C060	$C068	$C070	$C078
9	off	off	off	off	on	on	$C040	$C048	$C050	$C058
10	off	off	off	off	off	off	$C060	$C068	$C070	$C078
11	off	off	off	off	on	on	$C040	$C048	$C050	$C058
12	off	off	off	off	off	off	$C060	$C068	$C070	$C078
13	off	off	off	off	on	on	$C040	$C048	$C050	$C058
14	off	off	off	off	off	off	$C060	$C068	$C070	$C078
15	off	off	off	off	on	on	$C040	$C048	$C050	$C058
16	off	off	off	off	off	off	$C060	$C068	$C070	$C078

The memory mapping for Turbo UMAC models allows for a total of 8 encoder channels to be selected. The dipswitch selects between only 2 base addresses. This allows for up to 2 ACC-51Es to be logically configured.

When using a slot addressable backplane, the repeated entries in the table above indicate the addresses that are applied at each slot.

Jumper E1 should be placed in the TURBO (1-2) select mode for MACRO Station processors that are revision 5 and higher. Older revision MACRO Station processors (revision 4 and lower) should have jumper E1 in the MACRO position (2-3).

NOTE

The ACC-51E defines the mapping for its encoder channels as the same as the mapping for other devices that provide encoder inputs. Therefore, although there are 2 - four channel memory "slots" to place the ACC-51E into, these same "slots" are shared with backplane axis cards. "Stack" style 2 axis cards do not have conflicts with the ACC-51E.

Jumper Configurations

Table of Jumpers

Nomenclature	Physical Layout	Description	Factory Default
E1	1 - 2 - 3	MACRO station / TURBO Select 1 - 2 Turbo UMAC Controller & MACRO Station Controllers (Rev 5 & up) 2 - 3 MACRO Station Controller (Rev 4 & older)	1 - 2
E2, E3, E4	1 - 2 - 3	Channel 1 Encoder Termination 1 - 2 Unterminated inputs 2 - 3 Terminated (120Ω) inputs (E4 is index termination)	2 - 3
E5, E6, E7	1 - 2 - 3	Channel 2 Encoder Termination 1 - 2 Unterminated inputs 2 - 3 Terminated (120Ω) inputs (E7 is index termination)	2 - 3
E8, E9, E10	1 - 2 - 3	Channel 1 index capture 1 - 2 Channel 2 is selected 2 - 3 Index capture is selected	1 - 2
E11, E12, E13	1 - 2 - 3	Channel 3 Encoder Term (opt1) 1 - 2 Unterminated inputs 2 - 3 Terminated (120Ω) inputs (E4 is index termination)	2 - 3
E14, E15, E16	1 - 2 - 3	Channel 4 Encoder Term (opt1) 1 - 2 Unterminated inputs 2 - 3 Terminated (120Ω) inputs (E4 is index termination)	2 - 3
E17, E18, E19	1 - 2 - 3	Channel 3 index capture 1 - 2 Channel 4 is selected 2 - 3 Index capture is selected	1 - 2

E1 - MACRO Station / Turbo Select

This jumper allows the use of a MACRO Station processor on this UBUS accessory. Since the MACRO Station was developed prior to the UBUS, there was a subtle address bus change. This jumper provides for the addressing difference between both architectures.

E2, E3, E4, E5, E6, E7 - Encoder Input Select Channel 1 & 2

These jumpers allow the user to select which type of input loading to be used for the encoder. A 120Ω termination is selectable. The inputs are approx. 20kΩ when not terminated.

E8, E9, E10 - Index Capture Select for Channel 1

These jumpers allow the user to select whether channel 2 is used for an encoder input or index capture for channel 1.

Channel 2 is not used when channel 1 index capture is selected.

E11, E12, E13, E14, E15, E16 - Encoder Input Select (Option 1- add'l 2 channels)

These jumpers allow the user to select which type of input loading to be used for the encoder. A 120Ω termination is selectable. The inputs are approx 20KΩ when not terminated.

E17, E18, E19 - Index Capture Select for Channel 3 (Option 1- add'l 2 channels)

These jumpers allow the user to select whether channel 4 is used for an encoder input or index capture for channel 3.

Channel 4 is not used when channel 3 index capture is selected.

TURBO UMAC AND THE UBUS INTERPOLATOR

I-variables for Turbo UMAC Processor

Refer to the TURBO PMAC Software Reference Manual for a more detailed description of the use of the I-vars as described below.

To properly process the interpolator's data, there are several I-variables that must be set:

External Servo IC Enable Control I-var (I65)

I65 is used to establish the presence of the ACC51P's Servo IC in the Turbo PMAC.

The table below shows how to set the bits of I65 for the ACC51P. Note that the servo ICs are enabled 2 at a time.

ACC51P Interp SW1 Settings				Turbo PMAC Servo IC # (m)	I65 Bit #	Bit Value
4	**3**	**2**	**1**			
on	on	on	on	2	0	1
on	on	on	off	3	0	1
on	on	off	on	4	1	2
on	on	off	off	5	1	2
on	off	on	on	6	2	4
on	off	on	off	7	2	4
on	off	off	on	8	3	8
on	off	off	off	9	3	8

External Servo IC Enable Control I-var (I66)

I66 is used to establish the type of servo IC used in the ACC51P by the Turbo PMAC.

The table below shows which bits of I66 are cleared for the PMAC1-style servo IC used in the ACC51P. Note that the servo ICs are selected 2 at a time.

Set the corresponding bit to "0" for the ACC51P style Servo IC.

ACC51P Interp SW1 Settings				Turbo PMAC Servo IC # (m)	I65 Bit #
4	**3**	**2**	**1**		
on	on	on	on	2	0
on	on	on	off	3	0
on	on	off	on	4	1
on	on	off	off	5	1
on	off	on	on	6	2
on	off	on	off	7	2
on	off	off	on	8	3
on	off	off	off	9	3

Encoder Decode Control I-vars (I7mn0)

I7mn0 is used to establish encoder decoding. 'm' is the servo IC number as established by the ACC-51E Mapping table (in the previous section); 'n' is the channel number, which is the same as the encoder number (1-4) on the ACC-51E board. The encoder decode control I-var is set for each channel that an interpolator is connected to.

Refer to the ACC-51E mapping table described in the Dipswitch and Mapping section above for the servo IC number 'm' value.

A value of 7 is used as default for CCW x4 Quadrature decode. Changing the decode direction requires the operator to save the TURBO PMAC's parameters and perform a $$$ or cycle power.

NOTE

The user MUST reset the PMAC if the encoder direction has been changed. If the encoder direction is changed, but the PMAC is not reset encoder instability will result!

Motor xx Homing, Software Position Capture & Trigger Mode

Ixx97 is used to establish position capture (i.e. Index Position Input). This variable must be set to 1 to function as software index capture. Note that there is a background cycle delay (typically 2-3 mSec), which limits the accuracy of the capture.

There is a status flag that is addressed by Ixx25 that points to the address of the flags for software or index capture. If limit switches are used on the axis, Ixx25 must point to the address where the limit switches occur. If the encoder's index channel is desired for software based homing, and limit switches are used on the axis, the encoder's index signal must be physically cross wired to the same hardware channel input as the flags for this function to work! The location of the cross-wired index channel input is usually on the same accessory card where the limit flags are connected.

NOTE

As of the printing of this manual, hardware index capture is not available for the ACC-51E.

Encoder Servo Feedback I-vars

Servo feedback is established from the set of I-vars for each channel that is located at Ixx03 and Ixx04. These values are addresses that establish an encoder reference that is used by the servo feedback algorithms to maintain a motor's position.

The following encoder table addresses are suggested when they are set up from the procedure that is outlined in 'ENCODER CONVERSION TABLE' in the PMAC software manuals. Refer to the table below:

	Ixx03,Ixx04 Value	**Conversion Table 1st Line Entry**	**Conversion Table 2nd line Entry**	**Conversion Table 3rd line Entry**
PROCESSED ENCODER #1	$3501	I8000	n.a. (single-line entry)	
PROCESSED ENCODER #2	$3502	I8001	n.a.	
PROCESSED ENCODER #3	$3503	I8002	n.a.	
PROCESSED ENCODER #4	$3504	I8003	n.a.	

PROCESSED ENCODER #5	$3505	I8004	n.a.	
PROCESSED ENCODER #6	$3506	I8005	n.a.	
PROCESSED ENCODER #7	$3507	I8006	n.a.	
PROCESSED ENCODER #8	$3508	I8007	n.a.	
PROCESSED ENCODER #9	$350B	I8008=$FF8200	I8009=$78205	I8010=00
PROCESSED ENCODER #10	$350E	I8011=$FF8208	I8012=$7820D	I8013=00
PROCESSED ENCODER #11	$3511	I8014=$FF8210	I8015=$78215	I8016=00
PROCESSED ENCODER #12	$3514	I8017=$FF8218	I8018=-$7821D	I8019=00
PROCESSED ENCODER #13	$3517	I8020=$FF8310	I8021=-$78305	I8022=00

These addresses are actually the default addresses used by Turbo PMACs for single-line encoder table references that represent axis 1 through 8. Processed encoder 9 through 12 represent sample entries for a UBUS interpolator with SW1 settings selected for all switches on or configurable slot #1(refer to tables in the previous section).

NOTE

The encoder table addressing starts at memory location $3501. Turbo PMAC processes all table entries until it finds a ***first*** line entry set to 00 (unused). There *MUST NOT* be any address gaps between the first and last encoder table entry.

NOTE

Due to timing constraints with the interpolator's conversion processes, it is recommended that the interpolator's encoder conversion table entries be placed at the contiguous end of the table. The interpolator may place unnecessary wait states back to the Turbo PMAC's processor if the conversion table entries are placed at the beginning of the conversion table.

placed at the beginning of the conversion table.

Commutation Position I-vars (Ixx83)

The ACC51E contains a quadrature-based encoder register that may be used for commutation position. The PMAC2 does not use the ACC51's full interpolation to track a motor's position.

The number of commutation counts per pole revolution or linear scale distance is related to the pitch of the encoder's sinusoidal output multiplied by 4. Therefore, commutation appears to the PMAC2 as if it were a quadrature-based encoder.

The tables below show the addresses of the quadrature register in the ACC51E:

Interp SW1 Settings:		**6**	**5**	**4**	**3**	**2**	**1**	**UMAC SERVO IC 2**
	1st Intrp	on	on	on	on	on	on	

ACC51E Channel Address	**Ixx83 Value**
$78200	$78201
$78208	$78209
$78210	$78211
$78218	$78219

Interp SW1 Settings: **UMAC SERVO IC 3**

	6	**5**	**4**	**3**	**2**	**1**
2nd Intrp	on	on	on	on	on	off

ACC51E Channel Address	Ixx83 Value
$78300	$78301
$78308	$78309
$78310	$78311
$78318	$78319

Interp SW1 Settings: **UMAC SERVO IC 4**

	6	**5**	**4**	**3**	**2**	**1**
5th Intrp	on	on	on	off	on	on

ACC51E Channel Address	Ixx83 Value
$79200	$79201
$79208	$79209
$79210	$79211
$79218	$79219

Interp SW1 Settings: **UMAC SERVO IC 5**

	6	**5**	**4**	**3**	**2**	**1**
6th Intrp	on	on	on	off	on	off

ACC51E Channel Address	Ixx83 Value
$79300	$79301
$79308	$79309
$79310	$79311
$79318	$79319

Interp SW1 Settings: **UMAC SERVO IC 2***

	6	**5**	**4**	**3**	**2**	**1**
3rd Intrp	on	on	on	on	off	on

ACC51E Channel Address	Ixx83 Value
$78220	$79221
$78228	$79229
$78230	$79231
$7823C	$79239

Interp SW1 Settings: **UMAC SERVO IC 3***

	6	**5**	**4**	**3**	**2**	**1**
4th Intrp	on	on	on	on	off	off

ACC51E Channel Address	Ixx83 Value
$78320	$78321
$78328	$78329
$78330	$78331
$78338	$78339

Encoder Conversion Table

The encoder conversion table is a user configurable list of entries that may be assigned to different specific data processing inputs. The interpolator is assigned into the encoder conversion table as a *High Resolution Encoder Interpolator* when using PEWIN's executive program conversion table setup menu. This entry uses a method digit value (bit 16-23) of $Mxxxxx. This entry also requires the user to set bit 15 to indicate that the ACC51-E uses a PMAC2 style gate array. Refer to section 5 in the Turbo PMAC software reference for "ENCODER CONVERSION TABLE SETUP LINES" (I-vars I8000-I8191) for details.

NOTE

The Executive Program with release dates before 2ND quarter 2000 do not permit automated setup of the table in the "Configure Encoder Table" function. With older Executive Programs, the user must manually configure the encoder table using memory write commands.

The following table describes the three-line I8xxx variables that need to be configured for the UBUS Interpolator. Note that either the dipswitch is set or the backplane addressable slot is used:

Interp SW1 Settings: **4 3 2 1** **TURBO PMAC SERVO IC 2**

1st Intrp on on on on

Backplane slot #1

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning
I8xxx, I8xxx+1	$FF8200	$78205	$00	ACC-51E Encoder Ch 1
I8xxx+2, I8xxx+3	$FF8208	$7820D	$00	ACC-51E Encoder Ch 2
I8xxx+4, I8xxx+5	$FF8210	$78215	$00	ACC-51E Encoder Ch 3
I8xxx+6, I8xxx+7	$FF8218	$7821D	$00	ACC-51E Encoder Ch 4

Interp SW1 Settings: **4 3 2 1** **TURBO PMAC SERVO IC 3**

2nd Intrp on on on off

Backplane slot #2

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning
I8xxx, I8xxx+1	$FF8300	$78305	$00	ACC-51E Encoder Ch 1
I8xxx+2, I8xxx+3	$FF8308	$7830D	$00	ACC-51E Encoder Ch 2
I8xxx+4, I8xxx+5	$FF8310	$78315	$00	ACC-51E Encoder Ch 3
I8xxx+6, I8xxx+7	$FF8318	$7831D	$00	ACC-51E Encoder Ch 4

Interp SW1 Settings: **4 3 2 1** **TURBO PMAC SERVO IC 4**

5th Intrp on off on on

Backplane slot #5

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning
I8xxx, I8xxx+1	$FF9200	$79205	$00	ACC-51E Encoder Ch 1
I8xxx+2, I8xxx+3	$FF9208	$7920D	$00	ACC-51E Encoder Ch 2
I8xxx+4, I8xxx+5	$FF9210	$79215	$00	ACC-51E Encoder Ch 3
I8xxx+6, I8xxx+7	$FF9218	$7921D	$00	ACC-51E Encoder Ch 4

Interp SW1 Settings: **4 3 2 1** **TURBO PMAC SERVO IC 5**

6th Intrp on off on off

Backplane slot #6

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning

I8xxx, I8xxx+1	$FF9300	$79305	$00	ACC-51E Encoder Ch 1
I8xxx+2, I8xxx+3	$FF9308	$7930D	$00	ACC-51E Encoder Ch 2
I8xxx+4, I8xxx+5	$FF9310	$79315	$00	ACC-51E Encoder Ch 3
I8xxx+6, I8xxx+7	$FF9318	$7931D	$00	ACC-51E Encoder Ch 4

Interp SW1 Settings: **4** **3** **2** **1** **TURBO PMAC SERVO IC 2***

3rd Intrp on on off on

Backplane slot #3

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning
I8xxx, I8xxx+1	$FF8220	$78225	$00	ACC-51E Encoder Ch 1
I8xxx+2, I8xxx+3	$FF8228	$7822D	$00	ACC-51E Encoder Ch 2
I8xxx+4, I8xxx+5	$FF8230	$78235	$00	ACC-51E Encoder Ch 3
I8xxx+6, I8xxx+7	$FF8238	$7823D	$00	ACC-51E Encoder Ch 4

Interp SW1 Settings: **4** **3** **2** **1** **TURBO PMAC SERVO IC 3***

4th Intrp on on off off

Backplane slot #4

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning
I8xxx, I8xxx+1	$FF8320	$78325	$00	ACC-51E Encoder Ch 1
I8xxx+2, I8xxx+3	$FF8328	$7832D	$00	ACC-51E Encoder Ch 2
I8xxx+4, I8xxx+5	$FF8330	$78335	$00	ACC-51E Encoder Ch 3
I8xxx+6, I8xxx+7	$FF8338	$7833D	$00	ACC-51E Encoder Ch 4

It should be noted that a 2 channel ACC-51E Interpolator (without OPT 1) uses 4-channel address field settings. 2 channel interpolators may not overlap 4 channel boundaries.

SW1 position #4 must always be on for Turbo PMAC products.

As a UBUS device, the interpolator input is seen as a whole number counter with 3 fractional digits. There are 32 sub-steps that occur per single whole number step. Each change of the data is seen by PMAC as 1/32 (0.03125) count. Since PMAC uses fractional arithmetic, the result will be accurate to 1/32 of a whole number step. Refer to the appendix section of this manual for information on how to display encoder position, which includes fractional data.

NOTE

The encoder channels in the ACC-51E interpolator are additional to AB digital quadrature inputs that are present on the PMAC's axis card channels. The digital encoder inputs on the axis cards are still available for dual feedback uses such as velocity feedback inputs or handwheel encoders.

Using the PMAC Executive

The PMAC executive program is ideal for setting up the encoder conversion table. There is a list of configuration options in the "CONFIGURE ENCODER TABLE" part of the executive.

Choose consecutive entries as desired for each encoder's configuration.

Select "High-Resolution Interpolator" as the conversion style.

Be sure that the correct encoder source channel number is also selected.

Note the address of the processed data reported in the upper-left portion of the window.

Download the new encoder table data to PMAC and select the "View All Encoder Entries" function to verify that your entries are correct.

When finished, close the "Configure Encoder Table" window and type "SAVE" to store your new encoder table data.

With the above process completed, you should notice the data from the interpolator appear in the position window (when Imn00=1).

Example: Turbo PMAC with ACC-51E for 2 encoders

Two '3-line' encoder table entries starting at the 9th line in the Encoder Conversion Table.

```
Turbo PMAC - I Variable     Turbo PMAC Memory Location
  I8008=$FF8200                 $3509
  I8009=$078205                 $350A
  I8010=$000000                 $350B           ;data for I103 & I104

  I8011=$FF8208                 $350C
  I8012=$07820D                 $350D
  I8013=$000000                 $350E           ;data for I203 & I204

  I103=$350B                ;position 1 feedback address
  I104=$350B                ;velocity 1 feedback address

  I203=$350E                ;position 2 feedback address
  I204=$350E                ;velocity 2 feedback address

  I7210=7                   ;channel 9 decode

  I7220=7                   ;channel 10 decode
```

UMAC MACRO STATION PROCESSOR AND THE UBUS INTERPOLATOR

There are two ways to establish a setup for the ACC-51E when it is used with the UMAC MACRO Station Processor.

METHOD 1: Assign ACC-51E into 4 axes

The easiest way to configure the interface requires that the ACC-51E appears as 4 axes to the MACRO station processor. When used in this configuration, there are I variables available for establishing the encoder decode control and position compare registers.

NOTE

Hiperface is not available if the ACC-51E is configured as axes on the MACRO station.

I-variables for UMAC MACRO Station Processor

Refer to the UMAC MACRO Station Software Reference for details about how to set the MI-Vars in the MACRO Station.

To properly process the interpolator's data, there are several I-variables that must be set in the UMAC MACRO Station:

MS{node},MI101 - MI108 Ongoing Position Source Address

MS{node},MI101 - MI108 is used to point to the MACRO Station's encoder table (see encoder conversion table section below) as referenced by MI-Vars MI120 - MI151.

The table below shows how these variables are established for the ACC-51E:

MI-Var	Motor Node	Value For ACC-51E
MI101	1st Motor	$0012
MI102	2nd Motor	$0015
MI103	3rd Motor	$0018
MI104	4th Motor	$001B

The encoder table entries for ACC-51E are 3 lines long. The table above shows how the first 4 axes might be assigned.

MS{node},MI910 Encoder/Timer n Decode Control

MS{node},MI910 is used to establish encoder decoding. 'node' is the MACRO Station's slave node number as established by the setting of SW1 on the UMAC MACRO CPU processor card. The encoder decode control I-var is set for each channel that an interpolator is connected to.

A value of 7 is used as default for CCW x4 Quadrature decode. Changing the decode direction requires the operator to save the UMAC MACRO Processor's parameters and perform a $$$ or cycle power.

NOTE

The user MUST reset the MACRO Processor if the encoder direction has been changed. If the encoder direction is changed, but the MACRO Station is not reset encoder instability will result!

Motor Homing, Software Capture

Motor Homing Capture is done in the MACRO Master controller. These are typically the PMAC2 Ultralite or the TURBO PMAC2 Ultralite.

NOTE

As of the printing of this manual, hardware index capture is not available for the ACC-51E.

PMAC2 Software Homing

Ix03, Ix25, I9n2, and I9n3 are set in the PMAC2 Ultralite to configure for software homing capture. Refer to the "PMAC/PMAC2 Software Reference" manual for the details of setting these I-variables.

Ix03 Notes

Only software homing position capture is available as of distribution of this manual and that bit 16 *must* be set to one in I-var Ix03 on the PMAC2 Ultralite. This register also contains the address of the position feedback register. For single encoder feedback applications, Ix04 is set to the same value as Ix03 (except bit 16 is always 0).

Ix25 Notes

Ix25 is set to the address of the flag inputs. This does not need to be the same address as Ix03. However, if the value of Ix25 is different from Ix03, the Index input on the ACC-5E must be wired to the channel that is pointed to by Ix25.

Ix25 is usually set to the same address as Ix03 except when limit switches are used (such as PLIM, MLIM, HOMEFLG, USER).

I9n2 Notes

I9n2 is set to determine the kind of position triggering that will occur in the homing move. Set this value to 1 or 5 if only the index (channel C) of the encoder is used. The software reference provides the details for setting this variable.

I9n3 Notes

I9n3 is set only if I9n2 has a setting that involves flags (such as PLIM, MLIM, HOMEFLG, USER).

TURBO PMAC2 ULTRALITE Software Homing

Ixx03, Ixx24, Ixx25, Ixx97, I68n2, I7mn2, I68n3 and I7mn3 are set in the TURBO PMAC2 Ultralite to configure for software homing capture. Refer to the "TURBO PMAC2 Software Reference" manual for the details of setting these I-variables.

Ixx03 Notes

This register contains the address of the position feedback register. For single encoder feedback applications, Ix04 is set to the same value as Ixx03.

Ixx24 Notes

This register is default set by the TURBO ULTRALITE to $840001.

Ixx25 Notes

Ixx25 is set to the location of the flag inputs. This does not need to be the same location as Ixx03. However, if the value of Ixx25 is different from Ixx03, the Index input (encoder channel C) on the ACC-5E must be physically wired to the channel that is pointed to by Ixx25.

Ixx25 is usually set to the same address as Ixx03 except when limit switches are used (such as PLIM, MLIM, HOMEFLG, USER).

Ixx97 Notes

Ixx97 is used to establish position capture (i.e. Index Position Input). This variable must be set to 1 to function as software index capture. Note that there is a background cycle delay (typically 2-3 mSec), which limits the accuracy of the capture.

Encoder Conversion Table (in UMAC MACRO CPU)

The encoder conversion table is a user configurable list of entries that may be assigned to different specific data processing inputs. The interpolator is assigned into the encoder conversion table inside the UMAC MACRO CPU. This entry uses an encoder method digit value (bit 16-19) of $Fxxxx. Refer to the description of I-Vars MI120-MI151in the UMAC MACRO Station Software Reference for "ENCODER CONVERSION TABLE ENTRIES" (I-vars I8000-I8191) for details.

NOTE

The UMAC MACRO CPU has the encoder conversion table that is located inside the MACRO station. The actual data conversion is performed inside the station and gets shifted to the appropriate MACRO

registers as feedback to the PMAC2 Ultralite controller. The encoder table in the PMAC Ultralite controller usually needs no modification from factory default values to receive data from a MACRO Station.

The following table describes the three-line MI-vars that need to be configured for the UBUS Interpolator. Note the dipswitch configuration: addressable backplane is not allowed for UMAC MACRO Station systems…

Interp SW1 Settings: **4** **3** **2** **1** **CS2**

1st Intrp off off on on

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning
MI120,MI121,MI122	$F0C040	$C045	$00	ACC-51E Encoder Ch 1
MI123,MI124,MI125	$F0C048	$C04D	$00	ACC-51E Encoder Ch 2
MI126,MI127,MI128	$F0C050	$C055	$00	ACC-51E Encoder Ch 3
MI129,MI130,MI131	$F0C058	$C05D	$00	ACC-51E Encoder Ch 4

Interp SW1 Settings: **4** **3** **2** **1** **CS3**

2nd Intrp off off off off

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning
MI120,MI121,MI122	$F0C060	$C065	$00	ACC-51E Encoder Ch 1
MI123,MI124,MI125	$F0C068	$C06D	$00	ACC-51E Encoder Ch 2
MI126,MI127,MI128	$F0C070	$C075	$00	ACC-51E Encoder Ch 3
MI129,MI130,MI131	$F0C078	$C07D	$00	ACC-51E Encoder Ch 4

It should be noted that a 2 channel ACC-51E Interpolator (without OPT 1) uses 4-channel address field settings. 2 channel interpolators may not overlap 4 channel boundaries.

On the ACC-51E, SW1 position #3 and #4 must always be off for Turbo PMAC products. Jumper E1 (if present) should always be set to TURBO (pos 1 - 2) for proper address decoding.

As a UBUS device, the interpolator input is seen as a whole number counter with 3 fractional digits. There are 32 sub-steps that occur per single whole number step. Each change of the data is seen by PMAC as 1/32 (0.03125) count. Since PMAC devices use fractional arithmetic, the result will be accurate to 1/32 of a whole number step

NOTE

The encoder channels in the ACC-51E interpolator are additional to AB digital quadrature inputs that are present on the PMAC's axis card channels. The digital encoder inputs on the axis cards are still available for dual feedback uses such as velocity feedback inputs or handwheel encoders.

When dual feedback is used, the MI-Var values shown in the table above will be different.

METHOD 2: Set Registers Using MI198 and MI199

The general idea of this method is that you may set the registers in the ACC-51E to their proper values and not use up the 4 axes as they are used in METHOD 1 above. The ACC-51E may be mapped into an unused address space and manually configured.

Since it is possible to have a UMAC MACRO Station that has two 4-axis stack cards. It is possible to insert up to 2 ACC-51E cards into the MACRO station and not have any address conflicts. This will allow up to 8 axes with dual-encoder feedback to be used where each axis has a single quadrature encoder and also a sinusoidal encoder.

This method uses MI198 and MI199 and requires a startup PLC to be written in the PMAC2 Ultralite controller. Refer to the UMAC MACRO Station Software reference for the typical usage of these variables.

The values that are set into the registers do not need to be exactly what is referenced here, but to simplify the method of configuration, the values presented here are based upon defaults commonly used with the ACC-51 interpolators.

Configure UMAC MACRO Station MI-Vars for ACC-51E

MS{node},MI101 - MI108 Ongoing Position Source Address

MS{node},MI101 - MI108 is used to point to the MACRO Station's encoder table (see encoder conversion table section below) as referenced by MI-Vars MI120 - MI151.

The table below shows how these variables are established for the ACC-51E:

MI-Var	Motor Node	Value For ACC-51E
MI101	1st Motor	$0012
MI102	2nd Motor	$0015
MI103	3rd Motor	$0018
MI104	4th Motor	$001B

The encoder table entries for ACC-51E are 3 lines long. The table above shows how the first 4 axes might be assigned.

Encoder Conversion Table

To set up the MACRO Station for a single ACC-51E accessory card, the configuration in the following table might be chosen. This will locate the ACC-51E at a memory base address of $C060. This is the location of CS3- in the MACRO station's backplane address.

Interp SW1 Settings:		**4**	**3**	**2**	**1**	**CS3**
	2nd Intrp	off	off	off	off	

I-Var.	1st Line Setting	2nd Line Setting	3rd Line Setting	Meaning
MI120,MI121,MI122	$F0C060	$C065	$00	ACC-51E Encoder Ch 1
MI123,MI124,MI125	$F0C068	$C06D	$00	ACC-51E Encoder Ch 2

MI126,MI127,MI128	$F0C070	$C075	$00	ACC-51E Encoder Ch 3
MI129,MI130,MI131	$F0C078	$C07D	$00	ACC-51E Encoder Ch 4

This table is identical to the table described in method #1 above. The encoder conversion table in the MACRO Station must always be configured. Save the MACRO Station's EErom (type MSSAVx) to preserve the above table's data.

Configure Registers Inside the ACC-51E

To set up the registers in the ACC-51E accessory card, the data in the following table is recommended:

Register Address	Value	Description
X:$C064	$0038D2	Global Clock Control for Channels 1 - 4
X:$C065	$000007	Control Word for Channel 1
X:$C06D	$000007	Control Word for Channel 2
X:$C075	$000007	Control Word for Channel 3
X:$C07D	$000007	Control Word for Channel 4

Global Clock Control Word

X:$C064 IC Global Control Word.

X:$C064 bits 0-11 (is set similar to MI903)

X:$C064 bit 12 Phase Clock Direction (0=output, 1=input) (This must be 1 in ACC-51E)

X:$C064 bit 13 Servo Clock Direction (0=output, 1=input) (This must be 1 in ACC-51E)

X:$C064 bit 14 - 23, not used- Set to zeros

Control Word for Channels 1 - 4

X:$C065, $C06D, $C075, $C07D Channel n Control Word

Bits 0-3 Encoder Decode Control (is set similar to MI910):

00: Pulse and direction decode

01: x1 quadrature decode

10: x2 quadrature decode

11: x4 quadrature decode

Bits 2-3: Direction & Timer Control (ACC-51E uses 00 or 01 only to establish encoder direction)

00: Standard timer control, external signal source, no inversion

01: Standard timer control, external signal source, invert direction

10: Standard timer control, internal PFM source, no inversion (not used by ACC-51E)

11: Alternate timer control, external signal source (not used by ACC-51E)

Bits 4-23: Not used by the ACC-51E (Set these values to 0)

NOTE

The ACC-51E uses a DSPGATE1 gate array device. A more detailed description of the registers may be obtained from the PMAC software reference manuals.

Configure Registers Inside the UMAC MACRO Station Processor

There is a single parameter per channel that must be poked into the MACRO Station processor's registers, this data is dependent upon the direction that was set in the control word when configuring the ACC-51E registers.

Put the data that is copied into the control word for each channel into the X register of the first encoder table entry for the channel used.

The chart below indicates where the encoder table entries MI120 - MI151 are pointing to in the UMAC MACRO station's memory map:

MI-Var.	Address	MI-Var.	Address	MI-Var.	Address	MI-Var.	Address
MI120	$0010	MI128	$0018	MI136	$0020	MI144	$0028
MI121	$0011	MI129	$0019	MI137	$0021	MI145	$0029
MI122	$0012	MI130	$001A	MI138	$0022	MI146	$002A
MI123	$0013	MI131	$001B	MI139	$0023	MI147	$002B
MI124	$0014	MI135	$001C	MI140	$0024	MI148	$002C
MI125	$0015	MI136	$001D	MI141	$0025	MI149	$002D
MI126	$0016	MI137	$001E	MI142	$0026	MI150	$002E
MI127	$0017	MI138	$001F	MI143	$0027	MI151	$002F

If the base address of the encoder conversion table entry is at MI120, then the value of the control word (recommended in the above section as $000007) should be poked into the MACRO Station processor's memory at X:$0010.

Example Program to Configure Registers MI198 & MI199

The following example shows a startup PLC that must be written in the PMAC Ultralite Master controller that will configure the registers needed to operate the ACC-51E.

This sample program will set the registers for 4 channels of sinusoidal encoder inputs that will appear at axes 1 through 4 on the UMAC MACRO Station controller. The controller should not be configured to include the ACC-51E interpolator as 4 axes for this example to work correctly.

The dipswitches should be set per the 2nd Interp addressing as described in the table above.

```
OPEN PLC1 CLEAR

P1=$E8C064 MSW0,MI198,P1      ;Point to Global Clock Control Register.
P2=$0038D2 MSW0,MI199,P2      ;Put $38D2 into the register.

P1=$E8C065 MSW0,MI198,P1      ;Point to control word for channel 1.
P2=$000007 MSW0,MI199,P2      ;Put $07 into the register.
```

```
P1=$E8C06D MSW0,MI198,P1    ;Point to control word for channel 2.
MSW0,MI199,P2               ;Put $07 into the register.
P1=$E8C075 MSW0,MI198,P1    ;Point to control word for channel 3.
MSW0,MI199,P2               ;Put $07 into the register.
P1=$E8C07D MSW0,MI198,P1    ;Point to control word for channel 4.
MSW0,MI199,P2               ;Put $07 into the register.

P1=$E80010 MSW0,MI198,P1    ;Point to 1st 3-line entry in encoder conversion table (X side).
P2=$000007 MSW0,MI199,P2    ;Place control word here (must be the same as #1 above)
P1=$E80013 MSW0,MI198,P1    ;Point to 2nd  3-line entry in encoder conversion table (X side).
MSW0,MI199,P2               ;Place control word here (must be the same as #2 above)
P1=$E80016 MSW0,MI198,P1    ;Point to 3rd 3-line entry in encoder conversion table (X side).
MSW0,MI199,P2               ;Place control word here (must be the same as #3 above)
P1=$E80019,MSW0,MI198,P1    ;Point to 4th 3-line entry in encoder conversion table (X side).
MSW0,MI199,P2               ;Place control word here (must be the same as #4 above)

DISPLC1                     ;Run this PLC only once at startup or MACRO Station reset.
CLOSE
```

The above program makes the assumption that the UMAC MACRO Station is set to operate at node 0. Refer to the PMAC2 Software Reference or the Turbo PMAC2 software reference for the usage of the MSWx and MSRx commands.

This program needs to be executed only once at power-up or station reset in the UMAC MACRO Station.

HIPERFACE INTERFACE OPTION (OPT2)

The Hiperface interface option is designed to operate the digital portion of SINCOS and SINCODER devices from Stegmann Corporation. The High Resolution Interpolator with Hiperface option supports commands that apply to the motion needs of PMAC products. These commands include absolute position, encoder temperature, sine-output mux (sincoder), index on RS485 lines (sincoder), encoder reset, error status, and encoder type.

SINCOS Encoders

SINCOS encoders from Stegmann Corp. use a microcontroller inside their encoders to provide a serial link, which is capable of transferring data to and from the encoder without affecting the sinusoidal output. Depending upon the model of encoder, different parameters pertaining to absolute position (single or multi-turn), encoder temperature, encoder type, and presence of encoder may be determined.

Absolute position is returned with a resolution of 16,384 counts per revolution in the SCS/SCM 60 and SCS/SCM 70 encoders.

The SCM 60 and SCM 70 models are capable of multi-turn absolute position reporting of up to 4096 revolutions of 16,384 steps per revolution. They have absolute position counters that roll over at 67,108,864 counts.

The SCS 60 and SCS 70 models are capable of single-turn absolute position reporting of 16,384 steps per revolution. They have absolute position counters that roll over at 16,384 counts.

NOTE

An application for the SINCOS Hiperface interface option is PMAC's power-on position for establishing the commutation position in brushless servomotors. This application uses the SINCOS encoder models in single-turn configuration.

SINCODER Encoders

SINCODER encoders from Stegmann Corp. also use a microcontroller inside their encoders to provide a serial link, which is capable of obtaining data from the encoder without affecting the sinusoidal output. Parameters pertaining to encoder type, and presence of encoder may be determined on a SINCODER.

SINCODERs are also capable of changing the type of sinusoidal outputs that they provide. The power-up default output resolution is typically 1024 sine cycles per revolution. The SINCODER is capable of being switched into a mode that outputs 1 sine cycle per revolution.

The serial data line may be set to output the index pulse from the sincoder. This output, when selected, sets the RS485 digital output until the index mark is reached. The RS485 line drops low when the index pulse is reached inside the encoder.

How to Contact Stegmann Inc.

USA:
Ph: (937) 454-1956
Fx: (937) 454-1955
Web: http://www.stegmann.com

Europe: (Encoder Division)
Ph: +49-771-807-121
Fx: +49-771-807-100
Web: http://www.stegmann.de

Using HIPERFACE

Upon power-up the Hiperface interface will automatically perform a 'READ POSITION SHIFTED' command and leave its data in the output registers.

Hiperface is defined as a 32-bit protocol. Therefore, in the 24-bit PMAC environment there are 2 sets of 24-bit registers needed for Hiperface transactions.

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base + 2 address	24 LSB Bits of Result																							
	Don't Care																				Encoder Command Word			

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base + 3 address					Status Bits												8 MSB Bits of Result							

The diagrams above show how the 2 registers are used. By placing a command into the 8 LSBs of the first register all 4 encoders are commanded to respond.

> ***NOTE***
>
> All 4 encoders are commanded to respond when any one of the command registers receives a command. Therefore, it is only necessary to issue one command for all connected encoders.

Using M-variables for Hiperface (TURBO Processor Only)

When using a TURBO PMAC the Hiperface interface involves the use of 3 m-variables. A PLC program should be written that implements the transactions that are used with these m-variables.

If the base address of the ACC-51E is at $78200, assign the m-variables as follows:

FLAG m-variables

	TURBO UMAC
Channel 1	M10->y:$78203,16,1
Channel 2	M20->y:$78203,17,1
Channel 3	M30->y:$78203,18,1
Channel 4	M40->y:$78203,19,1

LSB Register m-variables

	TURBO UMAC
Channel 1	M11->y:$78202,24
Channel 2	M21->y:$7820A,24
Channel 3	M31->y:$78212,24
Channel 4	M41->y:$7821A,24

MSB Register m-variables

	TURBO UMAC
Channel 1	M12->y:$78203,0,8
Channel 2	M22->y:$7820B,,08
Channel 3	M32->y:$78213,0,8
Channel 4	M42->y:$7821B,0,8

Hiperface Register Operation

The flag M-variables are set to "1" while the Hiperface interface is performing the commanded operation. At the beginning of the commanded operation, the LSB Register is set to "000000" for the conversion.

When the commanded operation is complete, the LSB and MSB registers will contain data and the flag register will be set to "0".

If the flag register remains a "1" and the LSB register has a number other than "000000" then there is an error on that encoder's response.

Example Hiperface Program (for TURBO Processor)

For this example of the register interaction using the Hiperface interface, we will use channel 1.

The parameters m10 and m11 are variables as assigned above to represent the flag and LSB register values.

I5111 is a Turbo PMAC2 countdown timer that is used for a time loop that allows time for the Hiperface hardware to respond. I68 is normally set to its default value of 15 to allow I5111 to operate correctly.

Write a PLC that contains the following:

```
m10->y:$78203,16,1                  ;Assign status bits for 4 encoder channels.
m20->y:$78203,17,1
m30->y:$78203,18,1
m40->y:$78203,19,1

m11->y:$78202,24                    ; Assign LSB data word (24 bits) for 4 encoders.
m21->y:$7820A,24
m31->y:$78212,24
m41->y:$7821A,24

m12->y:$78203,0,8                   ;Assign MSB data word (upper 8 bits of 32 bit-
m22->y:$7820B,0,8                   ;   word) for 4 encoders.
m32->y:$78213,0,8
m42->y:$7821B,0,8

OPEN PLC1 CLEAR                     ; Open a program buffer.

M11= $52                            ; Command Hiperface to return the encoder type.

I5111=20                            ; Set timer register for 20 servo cycles timing.
WHILE( I5111 > 0 ) ENDW             ; Wait for Hiperface hardware to set variables.

While( m10 = 1 and m11=0 ) wait     ; Loop until conversion is complete

IF( m10=1 )                         ; Check for error condition (m11<>0).
        SENDS"ERROR - CODE = "      ; Send MSG if so.
        CMDS"m11"                   ; This is error number.
ELSE                                ; Not error, send the encoder type.
        P1=(m12*65536)+m11          ; Get the encoder type value from 32 bits of data.
        SENDS"Encoder type is "     ; Refer to descriptions below for encoder type-
        CMDS"p1"                    ;  data format.
ENDIF

                                    ; Perform command for encoder in channel 2.
IF( m20=1 )                         ; Check for error condition (m21<>0).
        SENDS"ERROR - CODE = "      ; Send MSG if so.
        CMDS"m21"                   ; This is error number.
ELSE                                ; Not error, send the encoder type.
        P2=(m22*65536)+m21          ; Get the encoder type value from 32 bits of data.
        SENDS"Encoder type is "     ; Refer to descriptions below for encoder type-
        CMDS"p2"                    ;  data format.
ENDIF

DIS PLC1                            ; Only let this PLC run once.

CLOSE
```

HIPERFACE Commands

Refer to the encoder's manual for the details of each Hiperface command.

The following commands are available for Hiperface Encoders:

SINCOS	SINCODER	VALUE	DESCRIPTION	4TH BYTE (8 BITS)	3RD BYTE (8 BITS)	2ND BYTE (8 BITS)	1ST BYTE (8 BITS)
✓		030h	Enc Temperature	00	00	Bits 8-15	Bits 0-7
	✓	038h	Set to 1024 Lines	00	00	00	00h
	✓	039h	Set to 1 line	00	00	00	01h
✓		03Fh	Read Position Shifted	Bits 24-31	Bits 16-23	Bits 8-15	Bits 0-7
✓		042h	Read Position	Bits 24-31	Bits 16-23	Bits 8-15	Bits 0-7
✓		043h	Set Position to 00	00	00	00	00
✓	✓	050h	Error Status	00	00	00	Value
✓	✓	052h	Encoder Type	RS485 mode	Enc Type	EErom Size	Channel
✓	✓	053h	Encoder Reset	00	00	00	00
	✓	054h	Set Index Output	00	00	00	00
	✓	05Fh	Set Index Perm	00	00	00	00

030h Encoder Temperature

This command returns a 16-bit value of encoder temperature in °C. Use the following equation to obtain the actual encoder temperature:

$$\text{Enc. Temp } (^{\circ}\text{C}) = \frac{\text{Digital value} + 40}{2048}$$

038h Set Sincoder to 1024 Line Mode

This command sets a sincoder's MUX to 1024 lines/revolution mode. This is the default value for the SINCODER at power-up. The value returned should be 00 in the LSB registers.

039h Set Sincoder to 1 Line Mode

This command sets a sincoder's MUX to 1 lines/revolution mode. The value returned should be 00 in the LSB registers.

03Fh Read SINCOS Absolute Position Shifted

This command returns the 32-bit absolute position counter value of the SINCOS encoder shifted by 4 bits. This function is required by the PMAC for proper data scaling when calculating power-on position. This command executes automatically at startup.

042h Read SINCOS Absolute Position

This command returns the 32-bit absolute position counter value of the SINCOS encoder.

043h Set SINCOS Absolute Position to Zero

This command resets the encoder's absolute position counter to a value of zero. The value of the return registers is set to zero.

050h Read Encoder Error Status Register

This command returns the value that is stored in an error register inside the Hiperface encoder. After reading, this register is reset to 00.

00h	NO ERRORs	
01h	Encoder analog signals are unreliable	
02h	Wrong synchronization or offset	
03h	Data field operations disabled	❶
04h	Analog monitoring inoperative	
05h,06h,07h	Internal hardware fault detected, encoder not operational	
08h	Counting register overflow	❶
09h	Transmitted parity is incorrect	
0Ah	Checksum of transmitted data is wrong	
0Bh	Invalid command code	
0Ch	Wrong number of data bytes sent	
0Dh	Illegal transmitted command argument	
0Eh	Selected field has READ ONLY status	❶
0Fh	Wrong access authorization specified	
10h	Data field definition error (field size is incorrect)	❶
11h	Specified field address not available	❶
12h	Selected field does not exist	❶
1Ch, 1Dh	Sampling error, encoder not operational	
1Eh	Permissible operating temperature exceeded	

❶ These error codes are related to functions that are not used by PMAC's Hiperface interface. They are provided here for reference purposes only.

052h Read Encoder Characteristics

This command returns the encoder's characteristics. There are four 8-bit data fields returned from this command. They are:

1st byte Channel
2nd byte EEPROM size
3rd byte Encoder type
4th byte RS485 mode

Channel - The number of optional analog inputs
EEPROM size - Encoder's built-in EEPROM size
(EEPROM size * 16) - 128 = EErom memory size in bytes
Encoder Type - Type of encoder:
Multi-turn = 07h
Single-turn= 02h
SINCODER = 12h
RS485 mode - Serial data mode
Should be E4h - 9600Baud, parity odd, 4.5mS timeout,
With 120Ω terminating resistor.

053h Reset Encoder

This command is used for reinitializing the encoder.

054h Set Sincoder to Index Output Temporarily

This command sets the SINCODER to apply a low signal to the RS485 digital output lines until an internal index mark is detected.

The low signal occurs approximately 6mS after the command is received at the SINCODER. The output will go to high level to show the index mark present for the duration of the active index mark location. When the SINCODER is removed from the index mark, the signal will go low for approximately 5mS and then revert back to the digital RS485 mode and await more Hiperface commands.

05Fh Set Sincoder to Index Output Permanently

This command sets the SINCODER to apply the index mark to the RS485 digital output lines.

The low signal occurs approximately 6mS after the command is received at the SINCODER. The output will go to high level to show the index mark present for the duration of the active index mark location.

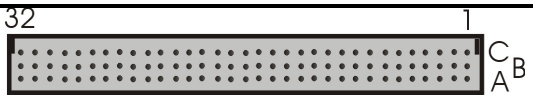
When power is removed from the SINCODER, it will revert back to the digital RS485 mode.

THINGS TO KNOW

1. Each sinusoidal cycle has 128 whole step quadrature transitions. There are always 32 fractional counts between quadrature transitions.
2. The fractional part of the interpolator's output is 0.03125 (1/32 count). PMAC products use fractional math so that fractional counts are part of motion calculations.
3. If your end product wants to use whole number counts for sinusoidal encoders, assign the motor using #1->32X to multiply the fractional counts into whole numbers. The executive program's position window may be adjusted to include the 32X scaling also.
4. The maximum sinusoidal input is approx. 1,400,000 SIN cycles/sec.
5. Be sure to use shielded, twisted pair cabling for sinusoidal encoder wiring. Double-insulated is the best. The sinusoidal signals are very small and must be kept as noise free as possible. Avoid cable routing near noisy motor or driver wiring! Refer to the appendix for tips on encoder wiring.
6. The use of single-ended output style sinusoidal encoders at very slow speeds has been shown to provide large amounts of velocity-ripple. When very slow speeds are desired, it is best to use differential output style sinusoidal encoders. The 3 line encoder table entry (which is available with Turbo PMAC models) has been designed to help adjust the offsets that may be present with single-ended encoders.
7. The ACC-51E uses only voltage mode 1Vp-p encoders.
8. It is possible that noise may be reduced in the encoder lines of a motor-based system by the use of inductors that are placed between the motor and the amplifier. Improper grounding techniques may also contribute to noisy encoder signals.

CONNECTOR DESCRIPTIONS

P1: UBUS Interface Connector

(96 pin EURO-Connector)		 Front View on Accessory Card	
Pin #	**Row A**	**Row B**	**Row C**
1	+5Vdc	+5Vdc	+5Vdc
2	GND	GND	GND
3	BD01	DAT0	BD00
4	BD03	SEL0	BD02
5	BD05	DAT1	BD04
6	BD07	SEL1	BD06
7	BD09	DAT2	BD08
8	BD11	SEL2	BD10
9	BD13	DAT3	BD12
10	BD15	SEL3	BD14
11	BD17	DAT4	BD16
12	BD19	SEL4	BD18
13	BD21	DAT5	BD20
14	BD23	SEL5	BD22
15	BS1	DAT6	BS0
16	BA01	SEL6	BA00
17	BA03	DAT7	BA02
18	BX/Y	SEL7	BA04
19	CS3-	BA06	CS2-
20	BA05	BA07	CS4-
21	CS12-	BA08	CS10-
22	CS16-	BA09	CS14-
23	BA13	BA10	BA12
24	BRD-	BA11	BWR-
25	BS3	MEMCS0-	BS2
26	WAIT-	MEMCS1-	RESET
27	PHASE+	IREQ1-	SERVO+
28	PHASE-	IREQ2-	SERVO-
29	ANALOG GND	IREQ3-	ANALOG GND
30	-15Vdc	PWRGUD	+15Vdc
31	GND	GND	GND
32	+5Vdc	+5Vdc	+5Vdc

NOTE

This table represents the standard UBUS backplane connector. The gray boxes represent signals that are not connected on this accessory board.

J1 Programming Header (Option 2)

This 6-pin header is used by manufacturing to program the on-board processor.

J2 Programming Header

This 6-pin header is used by manufacturing to program the UMAC decoder chip.

J3,J4 Encoder Inputs

(14 pin Mini-Combicon)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	SIN+	Analog Input	Sinusoidal input+	
2	SIN-	Analog Input	Sinusoidal input-	
3	COS+	Analog Input	Cosine input+	
4	COS-	Analog Input	Cosine input-	
5	INDEX+	Input	Index input	Analog or TTL levels
6	INDEX-	Input	Index input	Analog or TTL levels
7	ENCPWR	Output	Encoder power	+5Vdc (from UBUS)
8	GND		Digital ground	
9	GND		Digital ground	
10	HOME	Input	Home Circuit	
11	HOMERET	Input	Home circuit return	This circuit return is connected to J3,J4,J5,J6
12	DATA+	I/O	RS485 digital +	Hiperface (Option 2)
13	DATA-	I/O	RS485 digital -	Hiperface (Option 2)
14	VREF	2.5V Output	A-D reference output	5KΩ output

J3 is for the first channel input and J4 is the second channel input to the UBUS interpolator.

J5,J6 Encoder Inputs (Opt 1)

(14 pin Mini-Combicon)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	SIN+	Analog Input	Sinusoidal input+	
2	SIN-	Analog Input	Sinusoidal input-	
3	COS+	Analog Input	Cosine input+	
4	COS-	Analog Input	Cosine input-	
5	INDEX+	Input	Index input	Analog or TTL levels
6	INDEX-	Input	Index input	Analog or TTL levels
7	ENCPWR	Output	Encoder power	+5Vdc (from UBUS)
8	GND		Digital ground	
9	GND		Digital ground	
10	HOME	Input	Home Circuit	
11	HOMERET	Input	Home circuit return	This circuit return is connected to J3,J4,J5,J6
12	DATA+	I/O	RS485 digital +	Hiperface (Option 2)
13	DATA-	I/O	RS485 digital -	Hiperface (Option 2)
14	VREF	2.5V Output	A-D reference output	5KΩ output

J5 is for the first channel input and J6 is the second channel input to the UBUS interpolator.

APPENDICES

Sinusoidal Encoder Wiring

Sinusoidal encoders operate on the concept that there are 2 analog signal outputs that have a profile that is 90 degrees out of phase. They are available with different drive characteristics, some of which are described below.

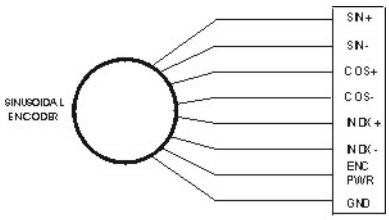
Differential Format

The differential format provides a means of using twisted pair wiring that allows for better noise immunity when wired into machinery.

There are two common output types available with differential style sinusoidal encoders. They are current mode and voltage mode style encoder output.

The current mode encoder output uses a high impedance 11µA pk-pk output. The voltage mode output encoder uses a low impedance 1 V pk-pk output.

The voltage mode encoder type is connected to the interpolator as shown. Termination is usually selected by using jumpers on the interpolator board.



DIFFERENTIAL ENCODER CONNECTION

NOTE

Voltage mode encoders are becoming the more popular choice for machine designs due to their lower impedance outputs. Lower impedance outputs represent better noise immunity, therefore more reliable encoder interfaces.

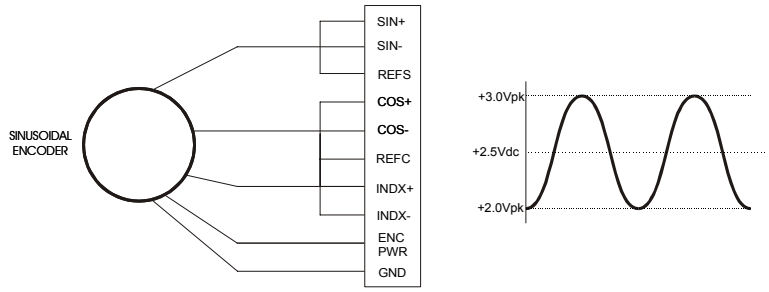
The ACC51P uses only voltage mode encoders.

Single-Ended Format

The single-ended formats provide a simpler means of using a sinusoidal encoder. Fewer wires are typically needed and the encoders are always of the lower impedance voltage output type.

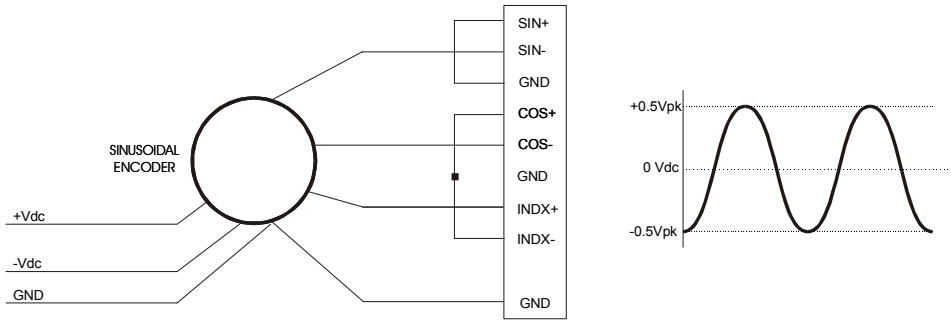
It should be noted that all the single-ended encoder formats shown here may have velocity-ripple effects at very slow speeds due to the effects of op-amp V_{io} offsets. These offsets cause the sinusoidal signal to be centered at a value that is slightly different than the reference or servo ground.

The diagram shown below is a simple single-ended encoder-wiring interface. This encoder has SIN and COS outputs that provide a 1-Volt peak to peak output that has a voltage offset of 2.5 Vdc. Note that the SIN-, COS-, and INDEX- lines are tied to the 2.5V internal references on the interpolator card.



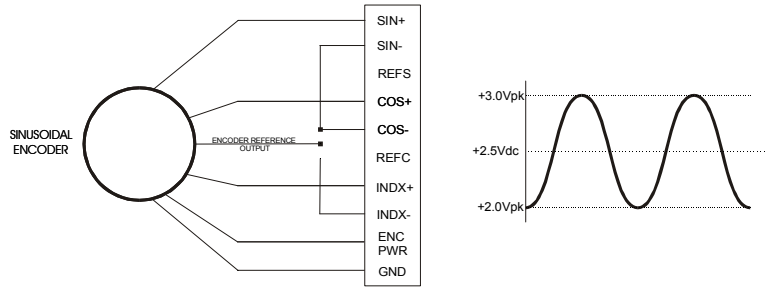
SINGLE-ENDED ENCODER CONNECTION

The diagram shown below is a similar to the diagram above. This encoder has SIN and COS outputs that provide a 1-Volt peak to peak output that has a voltage offset of 0.0 Vdc. Note that the SIN-, COS-, and INDEX- lines are tied to the GND on the interpolator card and the encoder usually requires a bipolar supply.



ALTERNATE SINGLE-ENDED ENCODER CONNECTION

The diagram shown below is a single-ended encoder that provides a reference output. This encoder has SIN and COS outputs which provide a 1 Volt peak to peak output that has a voltage offset which is provided as an output of the encoder. The SIN-, COS-, and INDEX- lines are tied to the encoder's reference output. This type of encoder connection is expected to be more precise than the typical single-ended encoder as shown in the first diagram above because the internal reference (usually set at 2.5Vdc) is the mechanism that establishes the offsets for the SIN+, COS+, and INDEX+ outputs.



SINGLE-ENDED ENCODER CONNECTION
USING THE ENCODER'S REFERENCE OUTPUT

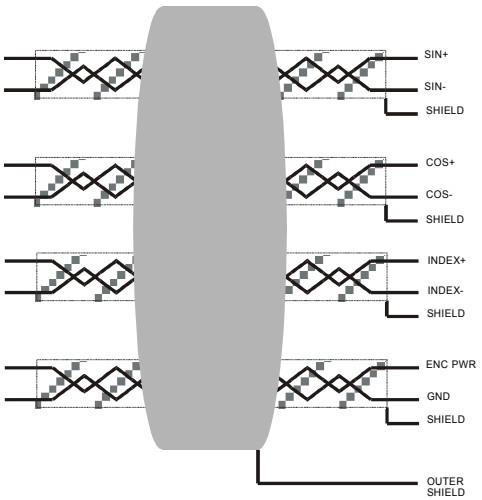
NOTE

Do not connect the reference output of the encoder to the REFS and REFC lines on the interpolator card. Doing so will cause the interpolator to function incorrectly.

Type of Cable for Encoder Wiring

Low capacitance shielded twisted pair cable is ideal for wiring differential encoders. The better the shield wires, the better the noise immunity to the external equipment wiring. Wiring practice for shielded cables is not an exact science. Different applications will present different sources of noise, which may require experimentation to achieve the desired results. Therefore the following recommendations are based upon some experiences that we at Delta Tau Data Systems have acquired.

If possible, the best cabling to use is a double shielded twisted pair cable. Typically there are 4 pairs used in a differential encoder's wiring. The picture below shows how the wiring may be implemented for a typical differential encoder using double shielded twisted pair cable.



EXAMPLE OF DOUBLE SHIELDED
4 TWISTED PAIR CABLE

The shield wires should be tied to ground (Vcc return) at the interpolator end. It is acceptable to tie the shield wires together if there are not enough terminals available. Keep the exposed wire lengths as close as possible to the terminals on the interpolator.

NOTE

It has been observed that there is an inconsistency in the shielding styles that are used by different encoder manufacturers.

Be sure to check pre-wired encoders to insure that the shield wires are ***NOT*** connected at the encoder's side. Shield wires should only be connected on one side of the cable.

If your encoder has shield wires that are connected to the case ground of the encoder, insure that the encoder and motor cases are sufficiently grounded and do not connect the shield at the interpolator end.

If your encoder has pre-wired double shielded cable that has only the outer shield connected at the encoder, then connect only the inner shield wires to the interpolator. Be sure not to mix the shield interconnections.

One possible cable type for encoders is Belden 8164 or ALPHA 6318. This is a 4-pair individually shielded cable that has an overall shield. This double shielded cable has a relatively low capacitance and is a 100Ω impedance cable.

Cables for single-ended encoders need to be shielded for the best noise immunity. Single-ended encoder types cannot take advantage of the differential noise immunity that comes with twisted pair cables.

NOTE

If noise is a problem in your application, careful attention must be given to the method of grounding that is used in your system. Amplifier and motor grounding can play a significant role in how noise is generated in a machine.

It is possible that noise may be reduced in a motor-based system by the use of inductors that are placed between the motor and the amplifier.

Offset Register Mapping Definitions

Most of the registers in the table below are located inside the DSPGATE1. Refer to the DSPGATE1 in the TURBO software reference under "PMAC2 I/O Control Registers for details on the use of these registers. The Hiperface option registers and the Ext ADC registers are not a part of DSPGATE1.

	ADDR	X -Memory	Y-Memory
1st Channel	Base + 00h	Status Word 1	Time Between Enc Counts (SCLKs)
	Base + 01h	Phase Raw Count 1	Time Since Last Enc Count (SCLKs)
	Base + 02h	Servo Count 1	24 LSBs (Hiperface)
	Base + 03h	Flag Position Capture 1	FLAGS + 8MSBs (Hiperface)
	Base + 04h	Global Clock Control 1-4	PWM C1
	Base + 05h	Control Word 1	Ext ADC_A
	Base + 06h	Enc Compare Auto Increment 1	Ext ADC_B
	Base + 07h	Enc Compare Value B1	Enc Compare Value B1
2nd Channel	Base + 08h	Status Word 2	Time Between Enc Counts (SCLKs)
	Base + 09h	Phase Raw Count 2	Time Since Last Enc Count (SCLKs)
	Base + 0Ah	Servo Count 2	24 LSBs (Hiperface)
	Base + 0Bh	Flag Position Capture 2	FLAGS + 8MSBs (Hiperface)
	Base + 0Ch	DAC Strobe Output Word 1-4	PWM C2
	Base + 0Dh	Control Word 2	Ext ADC_A
	Base + 0Eh	Enc Compare Auto Increment 2	Ext ADC_B
	Base + 0Fh	Enc Compare Value B2	Enc Compare Value B2
3rd Channel	Base + 10h	Status Word 3	Time Between Enc Counts (SCLKs)
	Base + 11h	Phase Raw Count 3	Time Since Last Enc Count (SCLKs)
	Base + 12h	Servo Count 3	24 LSBs (Hiperface)
	Base + 13h	Flag Position Capture 3	FLAGS + 8MSBs (Hiperface)
	Base + 14h	ADC Strobe Output Word 1-4	PWM C3
	Base + 15h	Control Word 3	Ext ADC_A
	Base + 16h	Enc Compare Auto Increment 3	Ext ADC_B
	Base + 17h	Enc Compare Value B3	Enc Compare Value B3
4th Channel	Base + 18h	Status Word 4	Time Between Enc Counts (SCLKs)
	Base + 19h	Phase Raw Count 4	Time Since Last Enc Count (SCLKs)
	Base + 1Ah	Servo Count 4	24 LSBs (Hiperface)
	Base + 1Bh	Flag Position Capture 4	FLAGS + 8MSBs (Hiperface)
	Base + 1Ch	PWM Freq/Dead time/PFM Width 1-4	PWM C4
	Base + 1Dh	Control Word 4	Ext ADC_A
	Base + 1Eh	Enc Compare Auto Increment 4	Ext ADC_B
	Base + 1Fh	Enc Compare Value B4	Enc Compare Value B4

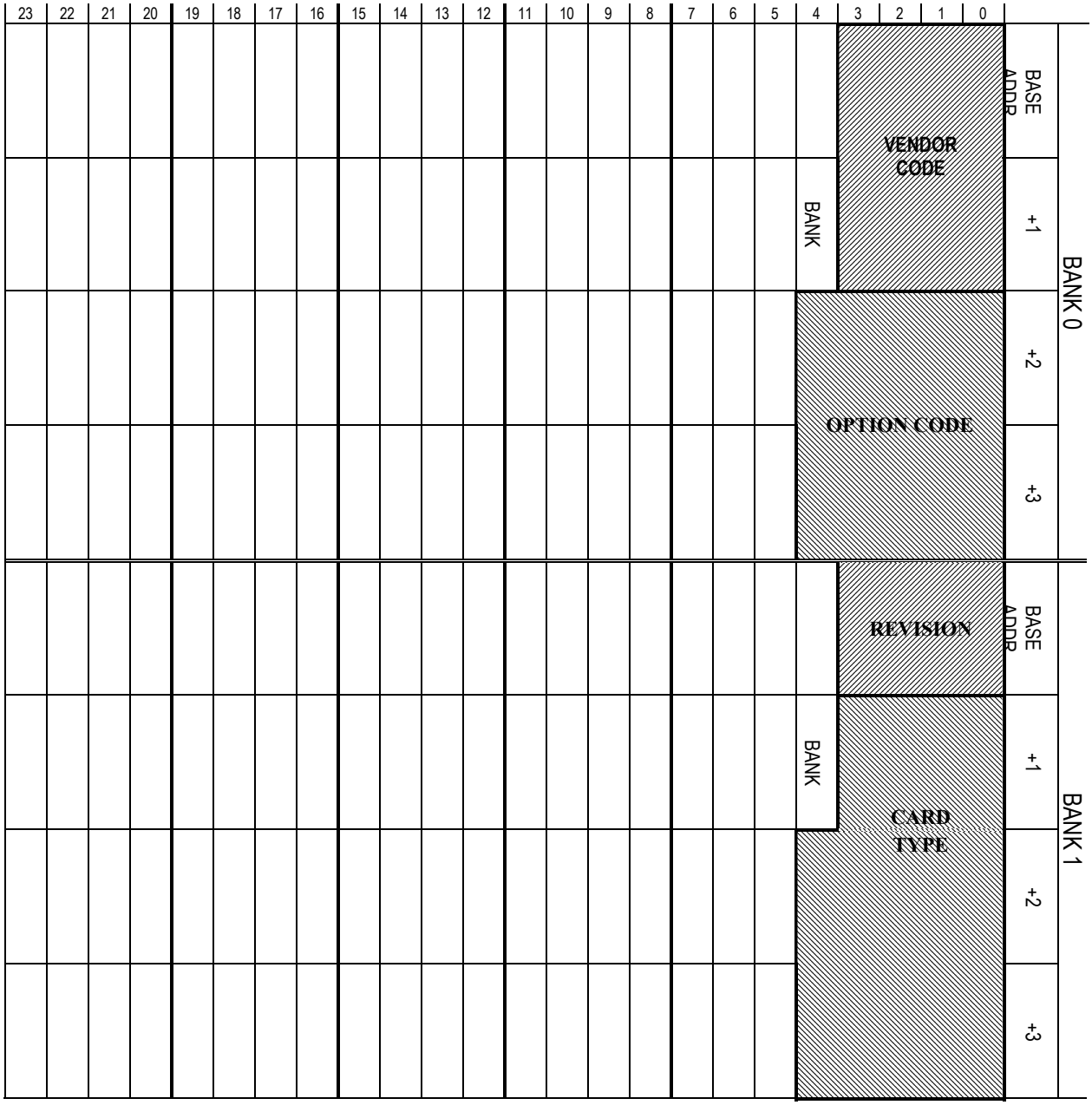
Ext ADC_A and Ext ADC_B are addresses to the same A-D converter. When accessed twice, the sine data is followed by the cosine data.

Board Configuration Memory Map

The board configuration memory mapping for Turbo UMAC models contains data pertaining to the configuration of products that are plugged into the UBUS backplane.

On power-up or at any time that is needed, the UBUS processor (normally a TURBO UMAC processor) is capable of polling this block of memory to establish the mapping of hardware.

Each block of memory contains 4 address locations that may be polled. There are 2 banks of 4 address locations that may be selected so that the processor may read data from up to 8 address locations.



BANK:

Place a 0 into this bit to select BANK 0. Place a 1 into this bit to select BANK 1.

VENDOR CODE:

Delta Tau Data Systems Inc. products will always have a 1 in this 4 bit address field. Products from other companies will have other values returned in this field.

OPTION CODE:

This 5 bit field contains data that pertains to options that are installed on the accessory card. Each product will have a different meaning to the data in this field.

REVISION:

This 4 bit field indicates the revision level the board assembly. This value is usually hard coded in the circuitry of the board fabrication.

CARD TYPE:

This 14 bit address field contains information pertaining to a part number assigned to the board. This value usually relates to a vendor's board assembly part number. Delta Tau Data Systems Inc. uses their 6 digit part number converted to hexadecimal in this field.

Option Codes:

The CS2 and CS3 selects that are used for the ACC-51E and axis cards allows for up to 16 board configuration slots to be used. The dipswitch selects between any of the 16 banks of memory. This allows for up to 16 ACC-51Es to be logically configured.

Home Flag Circuit

The circuit used for the home flag inputs is shown below for reference. This circuit is used when the home capture firmware is implemented (2nd Quarter 2000).